Matthew A. Taylor

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Education

Massachusetts Institute of Technology - B.S. in Electrical Science and Engineering

- **Current GPA:** 5.0/5.0
- **Graduation:** May 2026
- **Relevant coursework:** Analysis and Design of Digital Integrated Circuits, Digital Systems Lab, Signal Processing

Projects [https://github.com/MatthewATaylor]

FPGA Drum Machine [SystemVerilog, Python, cocotb, Vivado]

- Designed six real-time audio effects in fixed point with less than 1 ms total latency, including:
  - Resampling pitch shift (4 octave span) using a Farrow structure variable-rate upsampler and polyphase FIR downsampler
  - Virtual analog model of a 4-pole transistor ladder filter, including tanh feedback nonlinearity and oversampling
  - Algorithmic stereo reverb, consisting of 8 low-pass feedback comb filters and 4 all-pass filters per audio channel
- Verified fixed-point designs by directly comparing against floating-point Python code in simulation (cocotb testbenches)
- Developed memory interface to write/read audio samples and video data to/from DDR3 DRAM
- Developed UART interface to load audio samples and read MIDI data from an electronic drum kit

LED Dance Floor [SystemVerilog, C, Vivado]

- Wrote C software to decode animated GIF files and transmit data frames to an FPGA via Ethernet
- Developed an FPGA design to receive Ethernet data and interface with more than 11,000 RGB LEDs at 30 FPS

Modular Synthesizer [LTspice, KiCad]

- Designed analog spring reverb, envelope generators, voltage controlled (VC) oscillators, VC amplifiers, and VC filters
  - Modified historical designs to make use of more available components (e.g. replacing obsolete transistors)
  - Designed an improved transistor ladder filter to minimize attenuation at high Q factor
- Designed a real-time 8-channel MIDI interface (pitch, velocity, gate, CC) with Teensy microcontroller
- Verified circuit designs in LTspice and designed PCBs in KiCad for 13 total synth modules

Differential Amplifier Design and Tape-Out [Cadence Virtuoso, Intel 22 nm technology]

- Performed hand calculations to design current mirror biasing circuitry and determine the FinFET gate widths
- Verified the design with simulation in Cadence and demonstrated 29 dB gain at 1 MHz, exceeding the required specifications
- Designed an IC layout for the amplifier circuit following the Intel PDK guidelines

Experience

06/23-08/23 **Analog Devices** - FPGA Design Intern

- Implemented and evaluated an ASIC ADC design on an FPGA "digital twin" (SystemVerilog, Vivado)
  - Designed signal generators (sine, LFSR noise, etc.) in FPGA fabric for evaluating the ADC with various input conditions
  - Implemented a SPI interface for testing the ADC with external stimuli
  - Ensured timing closure and proper behavior at clock domain crossings (reset synchronizers, dual flip-flops, async FIFOs, etc.)
- Developed SystemVerilog testbenches to ensure state machines and signal processing logic matched specifications
- Wrote Python and TCL scripts to integrate the ASIC design in an automated build process
- Collaborated with an overseas team to develop an ADC evaluation setup on new measurement equipment

09/23-12/23 **Electrical Circuits: Modeling and Design of Physical Systems** - Lab Assistant

01/24-12/24 **MIT Palacios Group** - Undergraduate Researcher

- Improved a Verilog-A model for AlGaN/GaN HEMTs by incorporating temperature-dependent gate leakage (IWN 2024 first author)
- Assembled and tested a high-temperature DC/RF probe station to enable transistor measurements from 25°C to 1000°C

05/25-07/25 **National Renewable Energy Laboratory** - Summer Research Intern

- Developed an improved CdTe recombination modeling approach utilizing TRPL measurements and COMSOL simulation

Skills

- **HDL and Software Programming:** SystemVerilog, Verilog, cocotb, Python, C, C++, OpenGL
- **Interfaces and Protocols:** Ethernet, DRAM, HDMI, MIDI, UART, SPI
- **Design:** FPGA, PCB, timing closure, CDC, async FIFOs, analog and digital filters, fixed and floating point DSP
- **Tools:** Vivado, Cadence Virtuoso, LTspice, KiCad